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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,623	11/03/2003	Sterling Smith	MSS0009-US	3410

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EXAMINER	
LEE, SIU M	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,623	SMITH ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-31* is/are allowed.

6)☒ Claim(s) *1-3,5 and 6* is/are rejected.

7)☒ Claim(s) *4 and 7-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/3/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5-7 and 21-23 are objected to because of the following informalities:

(1) Claim 5, lines 5 and 9, replace "forth" with "fourth".

(2) Claim 6, line 2, replace "forth" with "fourth".

(3) Claim 7, line 2, replace "forth" with "fourth".

(1) Claim 21, lines 5 and 9, replace "forth" with "fourth".

(1) Claim 22, line 2, replace "forth" with "fourth".

(1) Claim 23, line 2, replace "forth" with "fourth".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 5,574,756) in view of Johansen et al. (US 6,538,475 B1).

(1) Regarding claim 1:

Jeong discloses a circuit comprising:

a clock generator (clock generator 22 and phase controller 24 in figure 2) for generating a first group of sampling clock pulses and a second group of sampling clock pulses for sampling an incoming data stream (clock generator 22 in figure 2 generates 4 clock signals CK0-CK3 as seen in figure 5A, column 6, lines 59-62), each sampling edge of said first group of sampling clock pulses and each sampling edge of said second group of sampling clock pulses being arranged alternatively and being separated from each other for an interval equal to half the period of said incoming data stream (clock generating circuit generates 2n clocks, each having 1/2n frequency of a maximum baud rate of data stream input and a phase difference of π/n between successive phases, abstract lines 1-4, CK0-CK3 each having the frequency and phase difference of π/2 between successive phase, the phase detector 18 selective completes the first discharge path, the third discharge path (first group) and the second discharge path and the fourth discharge path (2 group) in that order, column 7, liens 9-15, for an example of 4 clocks being generated, figure 5 shows the relationship between the clock signals and the data, each clock CK0-CK3 is separated by half of the period of the data), said clock generator being controlled in response to a phase control signal (the control signal form the phase detector 18 in figure 2, column 4, lines 40-53) to adjust phases of said first group of sampling clock pulses and said second group of sampling clock pulses (controller 24 shifting the respective phases of the clocks ahead or behind in response to the phase control signal, column 4, lines 18-20);

a data and phase sampling circuit (data sampler circuit 180 in figure 12) for receiving said incoming data stream (receives input data source 160 in figure 12), said

first group of sampling clock pulses and said second group of sampling clock pulses (data sample circuit 180 receives clock signal CK0-CK3 in figure 12), said data and phase sampling circuit taking samples of said incoming data stream in accordance with said first group of sampling clock pulses to produce a first sampled data stream while taking samples of said incoming data stream in accordance with said second group of sampling clock pulses to produce a second sampled data stream (the data sample circuit 180 generates data samples (OUT0-OUT3) according to the sample clocks CK0-CK3); and

a phase detection and correction circuit (phase detector 18 in figure 2) coupled to said data and phase sampling circuit.

Jeong fails to disclose for determining resemblances of each bit in said second sampled data stream to the corresponding two bits in said first sampled data stream, the associated sampling edge of said bit in said second sampled data stream being adjacent to the associated sampling edges of said two bits in said first sampled data stream, said phase detection and correction circuit producing said phase control signal on the basis of the resemblance determination result.

However, Johansen et al. discloses a phase detection and correction circuit (phase detector circuit in figure 4) coupled to said data and phase sampling circuit, for determining resemblances of each bit in said second sampled data stream (the sampled data SB from the D-FF 23 in figure 1, column 3, lines 54-57) to the corresponding two bits in said first sampled data stream (the sampled data SC from the D-FF 21 and the sampled data SA from the D-FF 22 in figure 1, column 3, lines 50-53), the associated

sampling edge of said bit in said second sampled data stream being adjacent to the associated sampling edges of said two bits in said first sampled data stream (SB is in the middle of SA and SC as shown in figure 1), said phase detection and correction circuit producing said phase control signal on the basis of the resemblance determination result (column 4, lines 39-51).

It is desirable for a phase detection and correction circuit coupled to said data and phase sampling circuit, for determining resemblances of each bit in said second sampled data stream to the corresponding two bits in said first sampled data stream, the associated sampling edge of said bit in said second sampled data stream being adjacent to the associated sampling edges of said two bits in said first sampled data stream, said phase detection and correction circuit producing said phase control signal on the basis of the resemblance determination result because it improves the jitter tolerance characteristic (column 2, lines 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Johansen et al. in the circuit of Jeong to improve the performance of the system.

(2) Regarding claim 2:

Johansen et al. further discloses that wherein said first sampled data stream is used as a data recovery output (the sampled data SA was sampled approximately at the center if the preceding bit period and sampled data SC was sampled approximately at the center of the present bit, therefore they are used as a data recovery output, column 3, lines 66-67 and column 4, lines 2-3).

(3) Regarding claim 3:

Jeong discloses that wherein said first group of sampling clock pulses and said second group of sampling clock pulses have the same frequency (from figure 5A, sample clock CK0-CK3 are of the same frequency, column 7, lines 9-11), which is equal to half the frequency of said incoming data stream (figure 5A and 5B show the relationship between the sample clocks CK0-CK3 and the DATA, the frequency of the sample clocks CK0-CK3 is half of the data (the period of the sample clocks CK0-CK3 are twice the period of the data)).

(4) Regarding claim 5:

Jeong discloses that wherein said first group of sampling clock pulses includes a first clock signal and a third clock signal and said second group of sampling clock includes a second clock signal and a fourth clock signal (the phase detector completes the first discharge path, the third discharge path, the second discharge path and the fourth discharge path in that order, column 7, lines 12-15), said first clock signal and said second clock signal being 90 degrees out of phase with each other (CK0-CK3 each having the same frequency and phase difference of $\pi/2$ between successive phases, column 7, lines 10-11), said first clock signal and said third clock signal being 180 degrees out of phase with each other (as shown in figure 5A, CK0 and CK2 is 180 degree out of phase, column 7, lines 10-11 indicates that the phase difference of $\pi/2$ between successive phases), and said second clock signal and said forth clock signal being 180 degrees out of phase with each other (as shown in figure 5A, CK1 and CK3 is 180 degree out of phase, column 7, lines 10-11 indicates that the phase difference of $\pi/2$ between successive phases).

(5) Regarding claim 6:

Jeong discloses that wherein rising edges of said first to said fourth clock signals are used as said sampling edges (column 6, lines 4-6).

Allowable Subject Matter

3. Claims 13-31 allowed.

4. Claims 4 and 7-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshioka (US 6,737,896 B2) discloses a synchronous circuit. Sugita (US 2003/0091136 A1) discloses a skew adjustment circuit, skew adjustment method, data synchronization circuit, and data synchronization method. Gutnik (US 7,183,864 B1) discloses a ring oscillator for use in parallel sampling of high speed data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee
2/28/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER